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14. ABSTRACT

This report was developed under a SBIR contract for topic **AF08-BT02**. Polaris Sensor and UNM developed a growth optimized DDWELL FPA and a novel ROIC which allows the bias voltage of individual pixels to be controlled independently. In one mode of operation, the bias voltages of neighboring pixels can be varied such that two or more IR color images are interlaced, much in the way a color camera employing Bayer color filters interlaces Red, Green and Blue colored images.

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Quantum Dot IR Photodetectors

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Draft Final Report

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TABLE OF CONTENTS

Section **Page**

List of Figures

Figure

List of Tables

Table **Page**

No Tables

1.0 SUMMARY

The goal of this program was to design and fabricate a ROIC that allows individually controllable pixel bias for DWELL Quantum Dot IR focal plane arrays (FPAs). Biasing the voltage of the detector modifies its spectral response. In this effort a DWELL Quantum Dot device was fabricated and tested. The results, shown in **Section 4.3** of this report, show that the spectral peak response can be shifted up to 2 microns in the LWIR portion of the spectra. The ROIC developed in this effort, allows the spectral response of pixels in the array to be adjusted arbitrarily. For example, in one mode of operation, the bias voltages of neighboring pixels can be varied such that two or more IR color images are interlaced, much in the way a color camera employing Bayer color filters interlaces Red, Green and Blue colored images. The ROIC enables the Quantum Dot focal plane array to operate as a spectrally agile sensor.

The effort was done in collaboration with Polaris Sensor Technologies and University of New Mexico (UNM). Polaris developed the unit cell for the ROIC design, UNM added additional circuitry to the design to allow testing and fabricated and tested the DWELL detector. At the time of the writing of this draft Final Report, the fabrication of the ROIC has not yet been completed. The reason for the delay is a large backlog in the foundry. The chip is being fabricated at MOSIS (http://www.mosis.com/), a low-cost prototyping and production volume service for VLSI circuit development. The ROIC chip is scheduled to be completed by 15 July 2012Payman, do we have a new date for the chip delivery Can we do the test before July 31st?. Testing will be completed by UNM and the results will be included in the Final Report before the Final Report deadline of 31Jul 2012.

This report shows the detailed design of the ROIC chip (**Section 4.1**), the test and validation ROIC chip (**Section 4.2**) and the design and measured performance of the DWELL Quantum Dot Detector (**Section 4.3**).

2.0 INTRODUCTION

Nanoscale infrared detectors are emerging as a potentially powerful alternative to traditional infrared detector technologies. The University of New Mexico has developed dots in well (DWELL) quantum dot infrared photodetectors which have a spectral responsivity that can be tuned by controlling the bias voltage applied. In this Phase II SBIR effort, Polaris Sensor and UNM designed a growth optimized DWELL FPA (designed and fabricated by UNM) and a novel ROIC (designed by Polaris, fabricated by MOSIS) which allows the bias voltage of individual pixels to be controlled independently. The bias voltage ranges possible with the ROIC from -5V to +5V permits a full spectral range of the quantum dot infrared detector. The format of the ROIC is 96 x 96 pixels with a 60 micron pitch. The spectral response tuning of the sensor built into the FPA itself provides a tremendous advantage over current multi-wavelength systems which rely on dispersive and refractive optics to obtain multiple spectral images. A multi-wavelength IR imager has a vast number of applications such as target detection in highly cluttered backgrounds, target detection and identification from fast moving platforms, detection of space threats, or plume signature determination. The multi-wavelength FPA has the potential to allow a small, compact and rugged multi-spectral IR imager.

This wavelength tunability can be exploited to perform multi-band sensing through an adaptive multispectral detector that can be simultaneously used in multiple bands in the mid-

wave and/or long-wave infrared (MWIR and LWIR). Recent advancements in the QDIP development have led to operation at higher temperatures, two color arrays (MWIR / LWIR operating at 80K), and arrays as large as 1Kx1K operating in the LWIR. The continuing development demonstrates that this technology may provide an alternative to more conventional HgCdTe and InSb IR FPAs.

3.0 METHODS, ASSUMPTIONS, AND PROCEDURES

Every detector in the detector array has an associated unit cell. The unit cell's function is to apply a programmable detector bias, integrate the detector's photocurrent, and sample the integrated value for subsequent output processing. The unit cell is composed of a detector bias sample and hold, a dual gain, capacitive transimpedance amplifier (CTIA), an output sample and hold, and a switched output buffer. Polaris Sensor Technology designed the unit cell that has this functionality. The University of New Mexico took the unit cell design and added circuitry including a PN junction underneath the chip to test and validate the functionality of individual cells. The assumption here is that testing the ROIC with this architecture is scalable to the bump bond process in which a DWELL detector array is bump bonded onto the ROIC for end to end testing. The testing protocol is done by testing the ROIC independently of the DWELL array. The DWELL is tested independently as well. Section 4.3 shows the design of the DWELL and the testing of the wavelength agility.

Because of delays in the fabrication of the ROIC device by MOSIS, those results will not available for the final report until approximately 30July 2012. Those results will be placed in Section 4.2 and the final report will be submitted at that time.

4.0 RESULTS AND DISCUSSION

In this section, we discuss the various electrochromic materials, their properties, and the modeling results.

4.1 ROIC Design

The high-level diagram for the individually controllable bias ROIC is shown in Figure 1, where the bias of each pixel is applied and set during the pixel readout process. For the first prototype and proof of concept, we chose to implement an array of 96x96 pixels that can be biased individually.

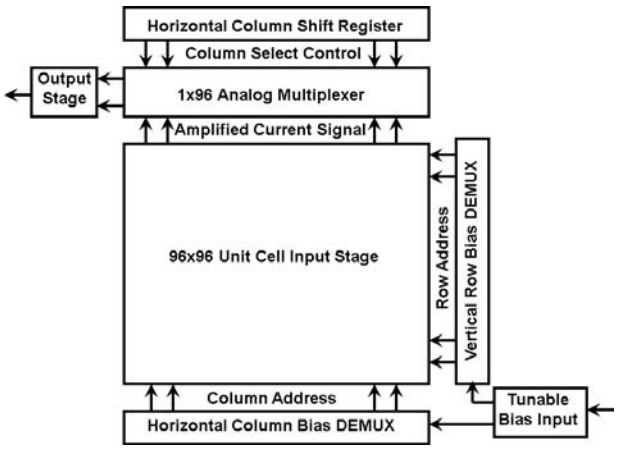


Figure 1 Basic building block of individually bias controllable ROIC

To fabricate the test chip, we have used TSMC's 0.35um high voltage CMOS through MOSIS. Prof. Zarkesh-Ha has established an infrastructure at his VLSI Design Lab at UNM to design and fabricate test chips through MOSIS.

The research activities carried out in this hardware design and implementation can be grouped into the unit cell design (Section 4.1.1), the supporting electronics (Section 4.1.2) and the readout electronics design (Section 4.1.3).

4.1.1 ROIC Unit Cell Design

Figure 2 shows the ROIC's unit cell schematics. Every detector in the detector array has an associated unit cell. The unit cell's function is to apply a programmable detector bias, integrate the detector's photocurrent, and sample the integrated value for subsequent output processing. The unit cell is composed of a detector bias sample and hold, a dual gain, capacitive transimpedance amplifier (CTIA), an output sample and hold, and a switched output buffer.

The detector bias sample and hold is located in the lower left hand corner of the unit cell schematics. It is constructed from a transfer gate, X1, and a poly/poly capacitor, XC4. The sampled bias voltage is applied to the detector (by way of the CTIA) during integration to tune it's spectral performance. Due to the CTIA's high input impedance, sample drift is relatively low, but periodic refreshing will be necessary.

The unit cell's capacitive transimpedance amplifier (CTIA) is used to integrate the detector's photocurrent. It is built around a differential amplifier, X3, shown in **Figure 3**. The detector bias sample is applied at the CTIA's noninverting input. The CTIA's feedback loop mirror's the bias voltage at the detector input to establish the desired detector bias level. Detector current entering the CTIA is routed through transfer gate, X2 during reset, and the CTIA's output voltage is held at the detector bias level. When X2 is disabled, the CTIA is taken out of reset, and integration of detector photocurrent commences. The CTIA gain is controlled via transfer gate X7. When X7 is enabled, the CTIA operates in the low gain mode, and all feedback capacitors are connected. If X7 is disabled, XC1 is the only active feedback capacitor, and the CTIA operates in high gain. Control voltages for X7 are provided by a single bit memory cell, X9. Schematics for the memory cell are shown in **Figure 5**.

The CTIA has a fixed output range. If one of the output rails is reached during integration, CTIA saturation will occur, and the bias voltage present at the detector input will begin to drift. This is due to the continued integration of photocurrent by the CTIA's feedback capacitance in the presence of a saturated output. High voltage damage of the detector or CTIA input stage can occur if this voltage drift isn't limited in some manner. MOSFET transistors M1 and M2 are configured as reverse biased diodes and connected to the CTIA's detector input. They safely limit the input voltage provide an alternate path for detector photocurrent in the event of CTIA saturation.

At the end of the integration period, an output sample and hold consisting of transfer gate X5 and poly/poly capacitor XC5 captures the integrated voltage. The CTIA is then placed back into reset in preparation for the next integration and readout cycle. The output sample is buffered by differential amplifier X4. Transfer gate X6 allows the buffered voltage to be placed on a ROIC column output bus during readout of the image frame.

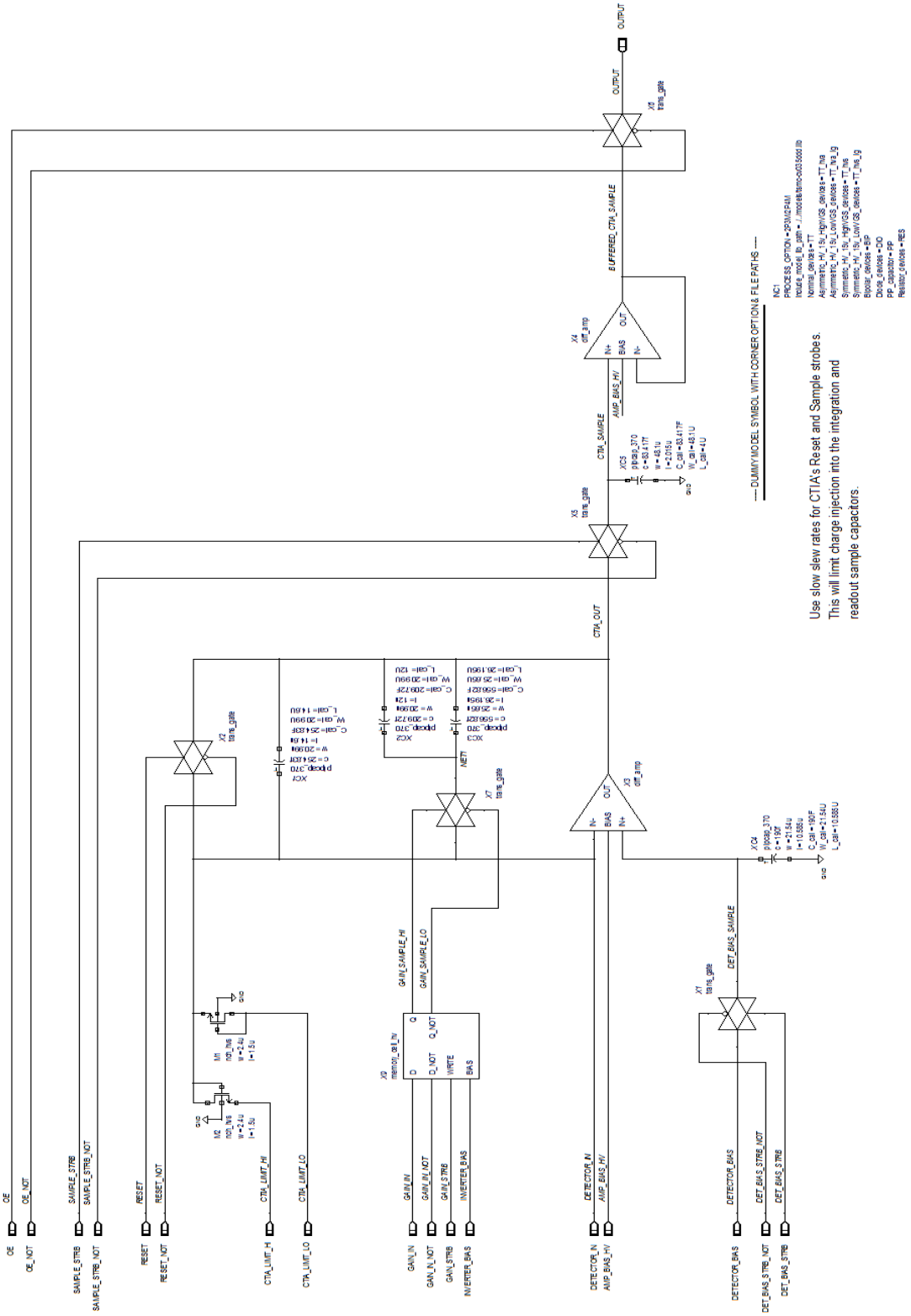


Figure 2 Unit Cell Schematic

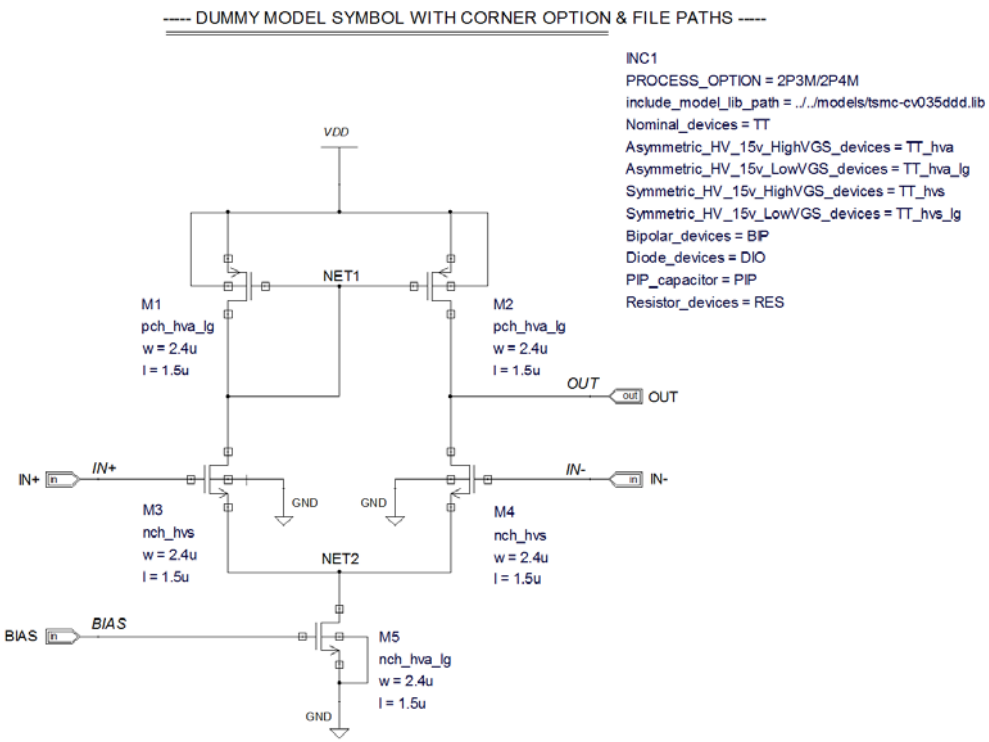


Figure 3 Differential Amplifier Used in CTIA and Output Sample Buffer

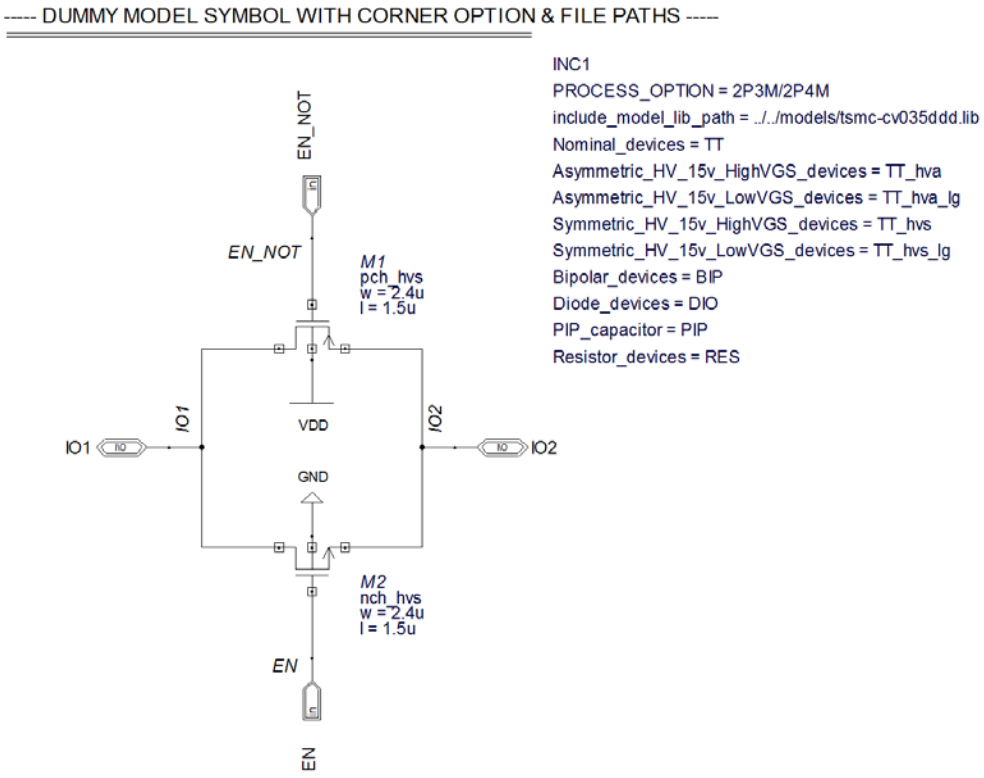


Figure 4 Transfer Gates Used to Switch Analog Signals

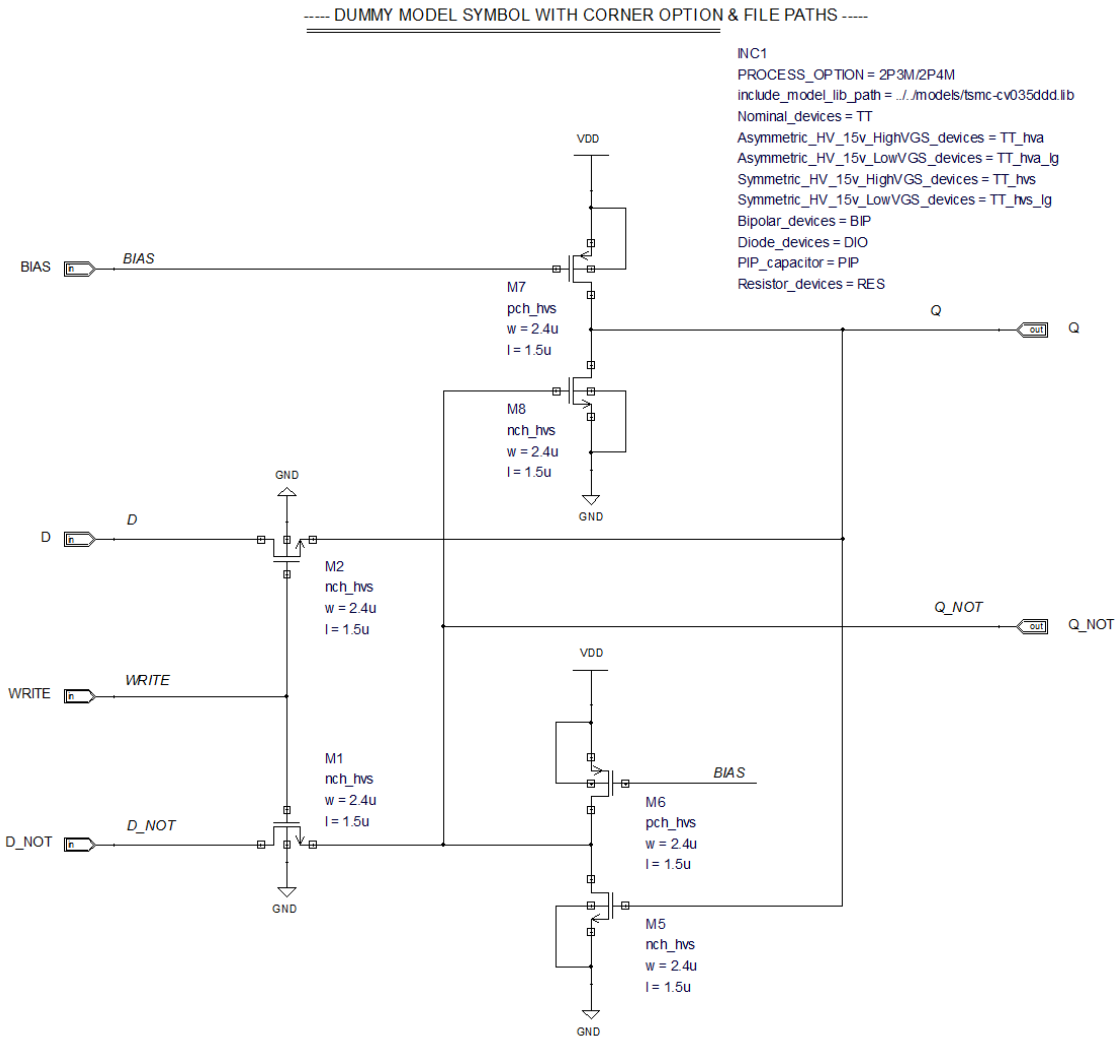


Figure 5 One Bit, High-Voltage Memory Cell Used To Store CTIA Gain.

Figure 6 shows the results of SPICE transient analysis performed to verify operation of the unit cell's CTIA and associated sample and hold buffers. The top trace shows the reset strobe used to clear the CTIA at the end of each integration period. The second trace shows the raw CTIA output prior to sampling. The third trace shows the sample strobe used to trigger sampling of the CTIA output, and the final trace represents the voltage measured at the CTIA's output sample and hold. A 1 nanoamp detector current is simulated, and the integration period has been set to 400 microseconds. In normal operation the CTIA would be held in reset while the FPA is readout. As stated earlier, the detector bias level for each unit cell is held in a local sample and hold. This level must be refreshed periodically to compensate for voltage drift due the leakage currents present in the sample and hold and op amp. The refresh rate necessary to maintain valid reference levels will be estimated using post layout SPICE models generated using Silvaco's Guardian net list extractor.

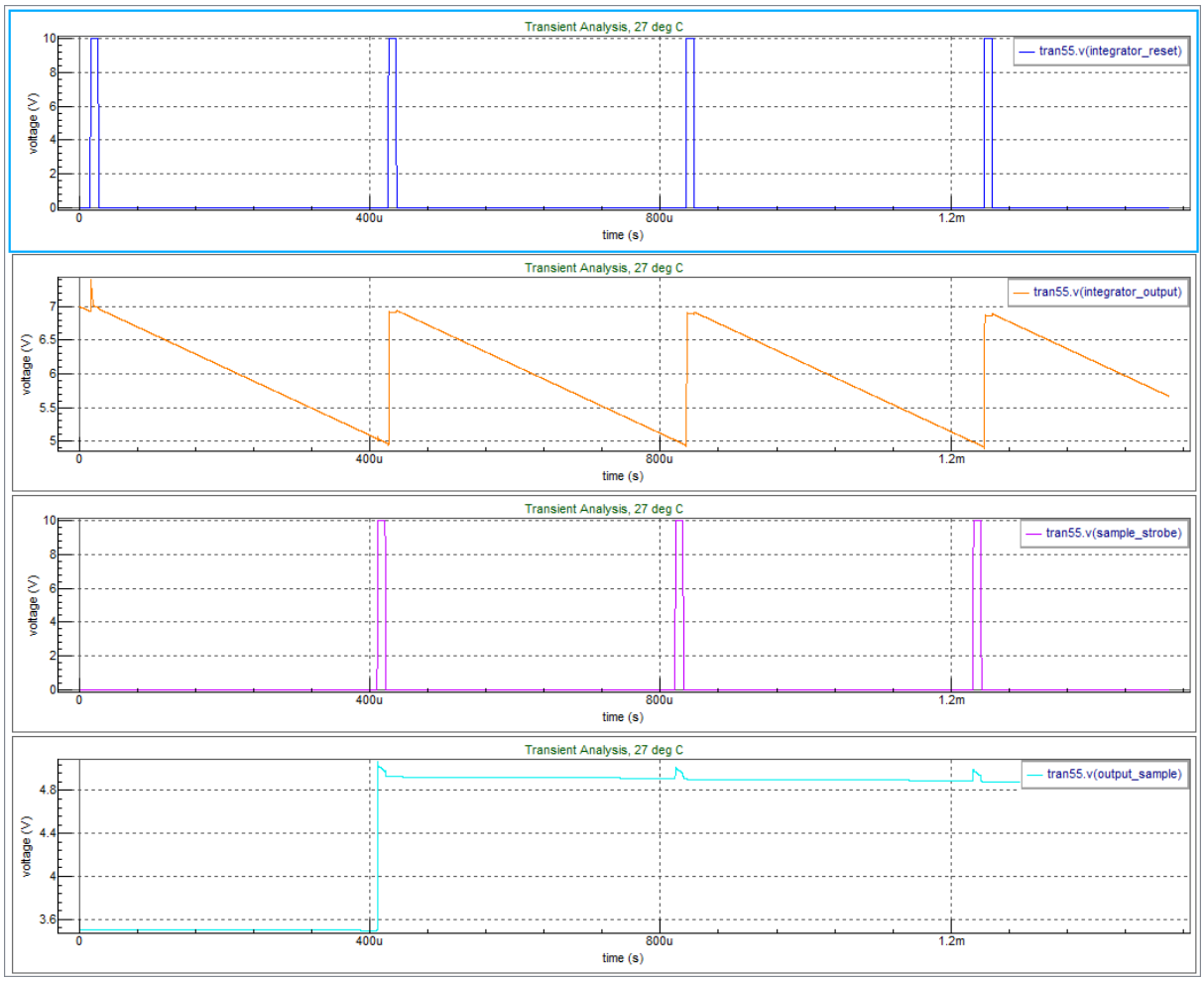


Figure 6 Unit Cell Transient Analysis

Figure 7 shows the final unit cell layout. The large, green rectangular regions are the sampling and integration capacitors; unit cell transistors are in the upper, right hand corner; and the unit cell bonding pad is the gray metallic region in the center of the layout. This cell measures 58 microns across which allows it to be replicated on a 60 micron pitch (please refer to **Figure 8**.)

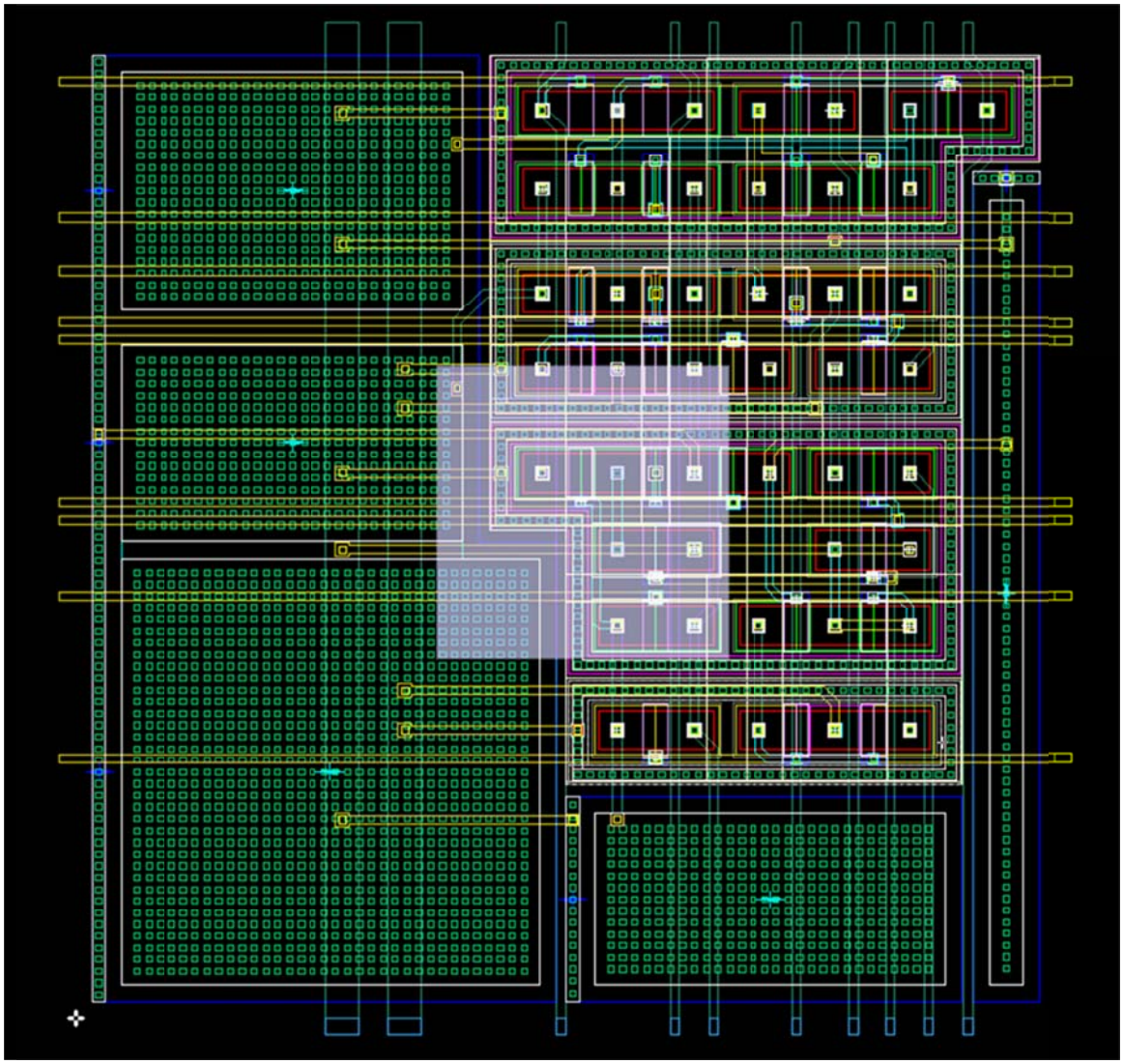


Figure 7 Unit Cell Layout

The original unit cell measured 45 microns across. This wasn't compatible with the University of New Mexico's detector array pitch of 30 microns. To accommodate the existing array pitch: the unit cell's capacitors were grown to result in the final layout dimension of 58 microns; the unit cell was replicated on a 60 micron pitch; and dummy bonding pads are inserted between active cell pads. The resulting unit cell array allows for the use of the original UNM detector array while providing programmable bias and reduced sample and hold drift. **Figure 8** shows a portion of the completed array.

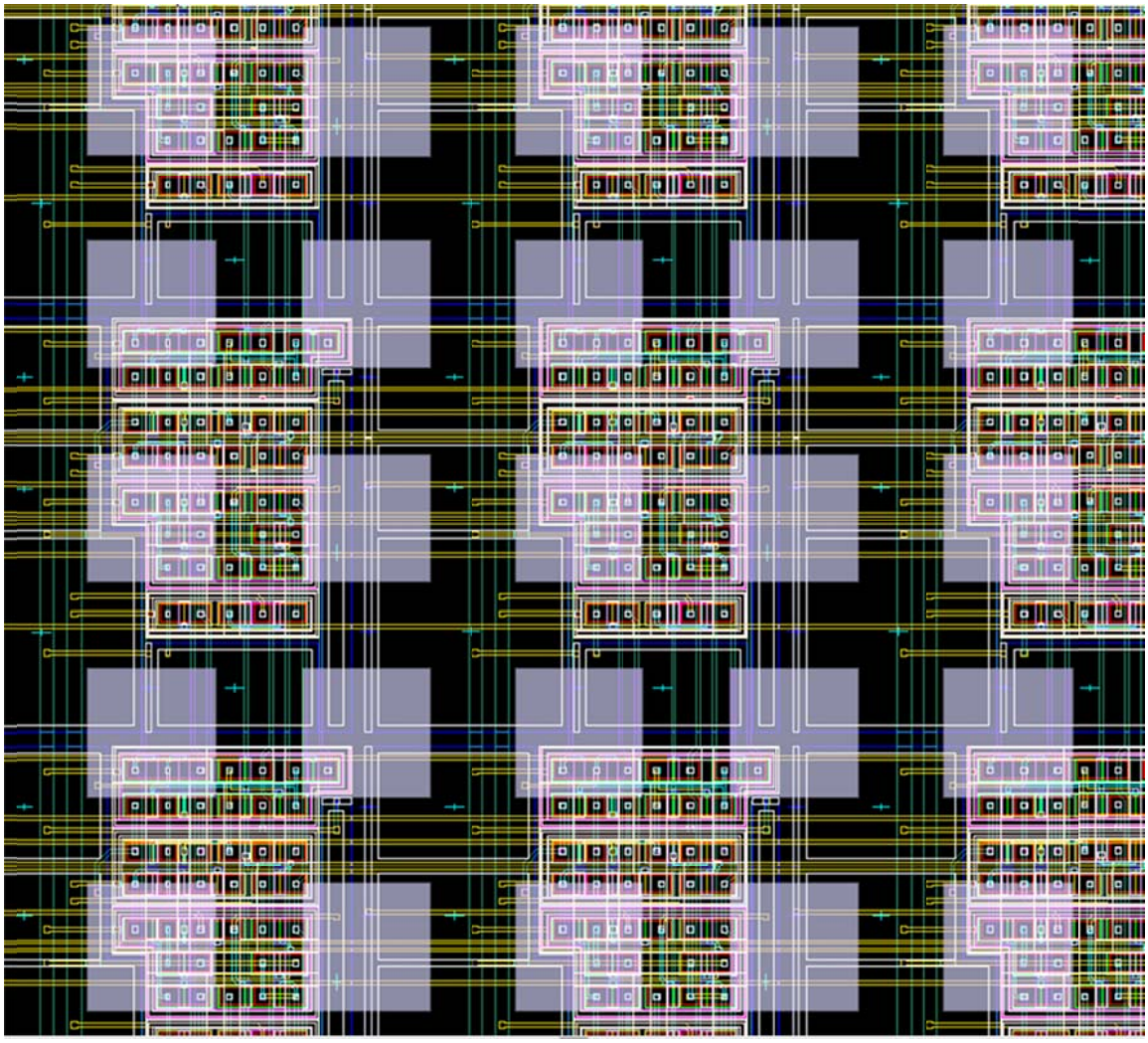


Figure 8 Portion of Unit Cell Array

4.1.2 Row/Column select design and other supporting circuits

The row select and column select blocks are responsible in synchronizing the pixel readout with clock, line sync (LSYNC), and frame sync (FSYNC) signals. We have used a special shift register to perform the row and column select as shown in **Figure 9**.

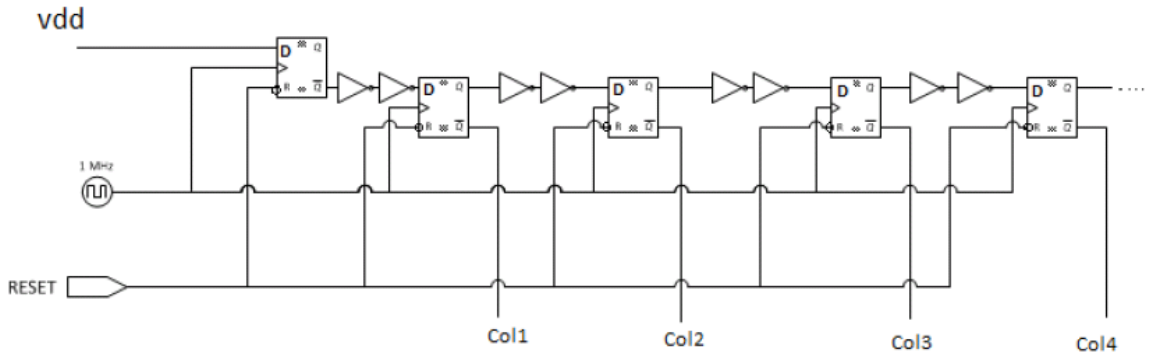


Figure 9 – The shift register used for row and column select circuits

The layout for the row select and column select as well as level shifter and the analog multiplexer circuits are shown in **Figure 10**. The pitch of these circuits must be designed to be precisely aligned with the unit cells.

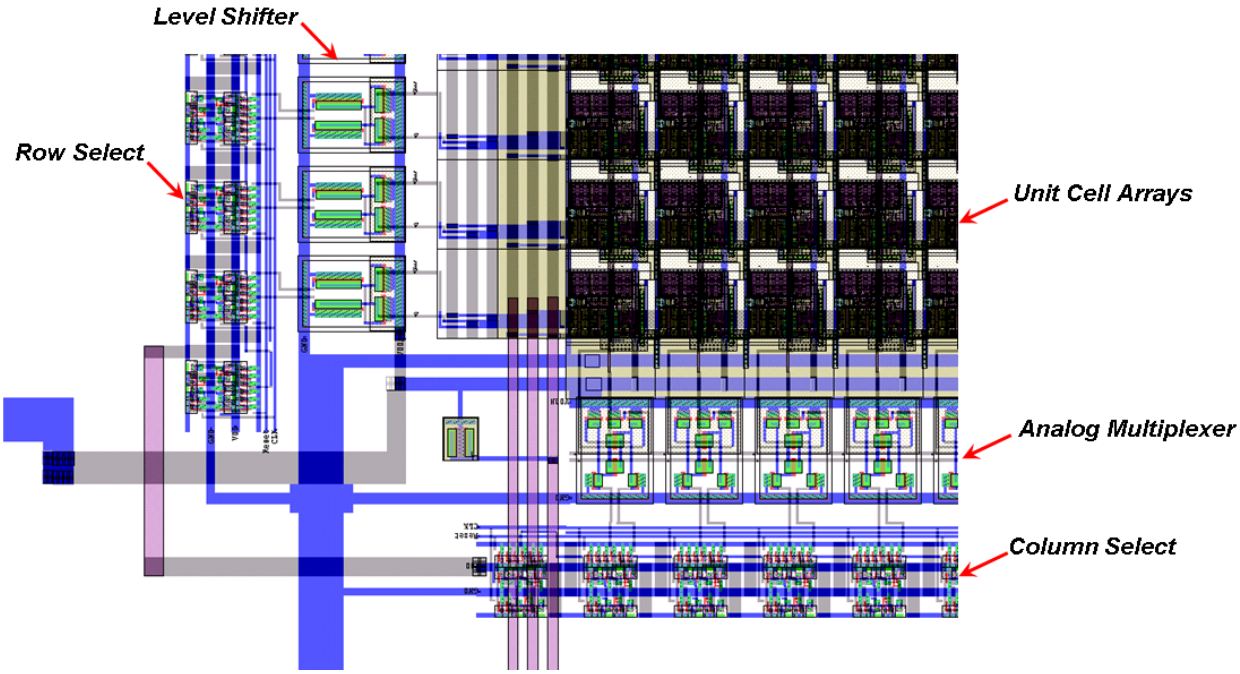


Figure 10 – The layout of the row/column select and other supporting circuits

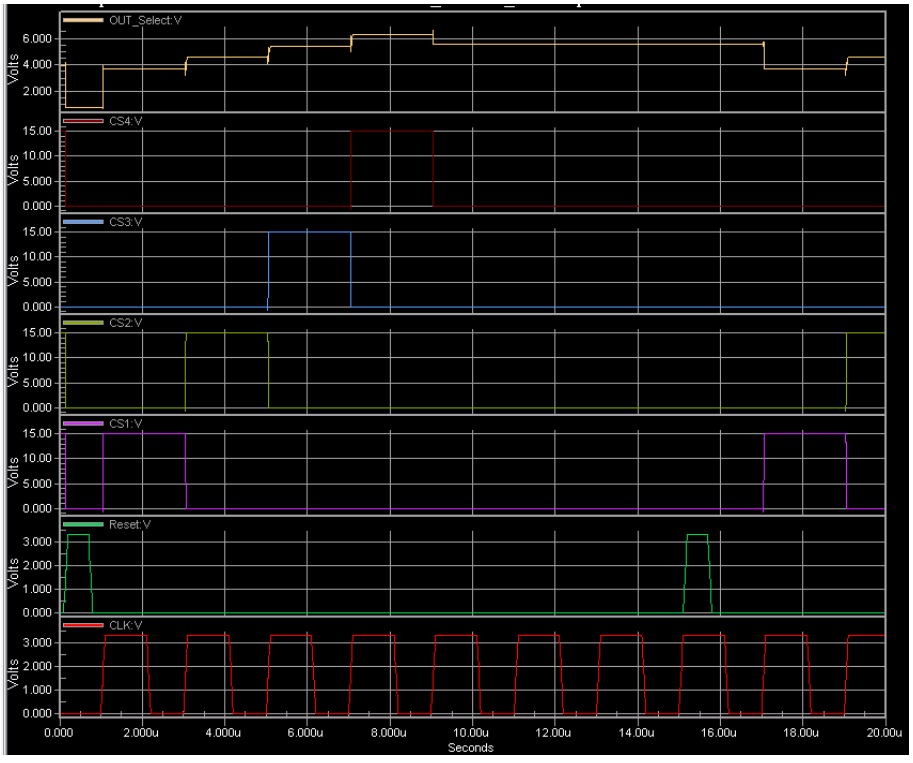


Figure 11– SPICE simulation results for multiplexer shown in Figure 10

Figure 11 shows the SPICE simulation result for the column select and the analog multiplexer is shown in **Figure 10**. As shown, after the reset and after each clock pulse, a column

is selected where its analog voltage is transferred to the output through the analog multiplexer. This simulation confirms the functionality of the column select, level shifter, and analog multiplexer used in this ROIC design.

The final test chip layout, which contains 96x96 arrays of individually controllable bias pixel, is shown in **Figure 12**. Each pixel includes a 30umx30um unit cell (CTIA, reset switches, output S&H, buffer, and bias S&H) and a PN photodiode for testing. The overall pixel size, including the unit cell and the photodiode is 40umx40um. The large area of the layout is dedicated for the pixel arrays. There are few additional test circuits for the main building blocks are also included on the periphery of the pixel arrays as shown in Fig. 9. The chip pad ring contains electrostatic discharge (ESD) devices for protecting the transistors in the core against electrostatic charge injection during chip handling. The chip is currently in the manufacturing process using TSMC's 0.35um HVCMOS fabrication through MOSIS.

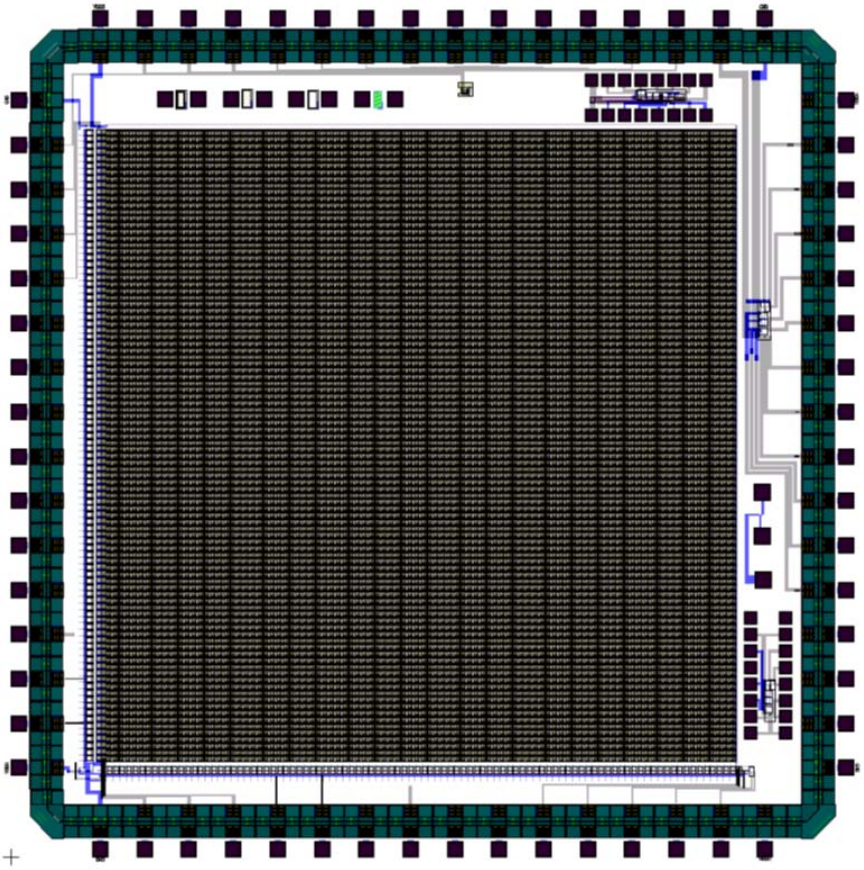


Figure 12 - The complete layout of the pixel-level controllable bias ROIC test chip

4.1.3 ROIC Control and Readout Electronics

The ROIC is designed to emulate a subset of the Indigo System's 9705 interface. It only supports full frame operation, but overlapping integration and frame readout periods are allowed. **Figure 13** shows a block diagram of the interface.

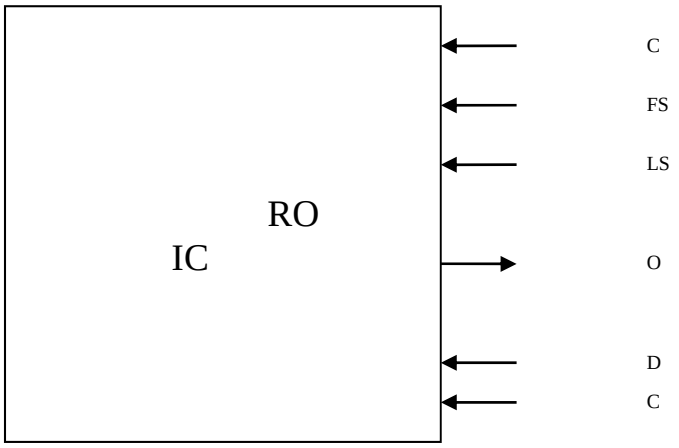


Figure 13 - ROIC Interface

The interface employs six I/O lines:

1. CLOCK: Master timing reference for all ROIC readout and control operations. It typically runs at 10 MHz

2. FSYNC: Digital input used to signal the start of each new frame and control unit cell integration timing.

3. LSYNC: Digital input used to control line readout timing.

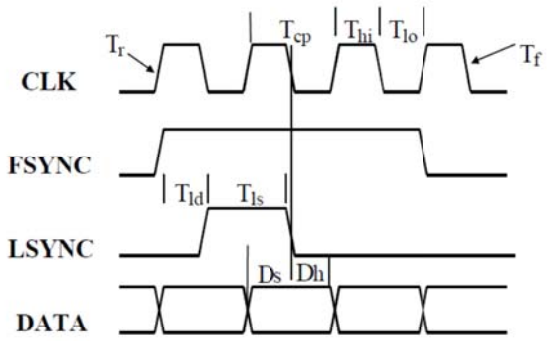
4. OUTPUT: Multiplexed analog output used to transmit image data during frame readout.

5. DET-BIAS: Multiplexed analog input used to configure detector bias levels during frame readout.

6. CTIA-GAIN: Multiplexed digital input used to configure integration gain levels during frame readout.

OUTPUT, DET-BIAS, and CTIA-GAIN are synchronized during readout. Each unit cell in the ROIC array has its detector bias level and integration gain refreshed while its analog output is being accessed.

Figures 14 through **18** provide the timing details associated with frame readout.



Parameter	Min	Typ	Max	Comments
T_r	-	-	10ns	10-90% (All signals)
T_f	-	-	10ns	90-10% (All signals)
T_{sh}	5ns	-	-	Setup / Hold Time: All Signals to CLK Edge
T_{cp}	200ns	-	-	10MHz Pixel Rate
T_{hi}	-	$.5*T_{cp}$	-	Clock Duty Cycle = 50%
T_{lo}	-	$.5*T_{cp}$	-	Clock Duty Cycle = 50%
T_{ls}	-	$1*T_{cp}$	-	LSYNC Width = 1 Clock Cycle min.
T_{ld}	$.5*T_{cp}$	-	-	FSYNC to LSYNC Delay
Ds	15ns	-	-	Data to CLK falling edge
Dh	15ns	-	-	Data to CLK falling edge

Figure 14 - Input Clock Details

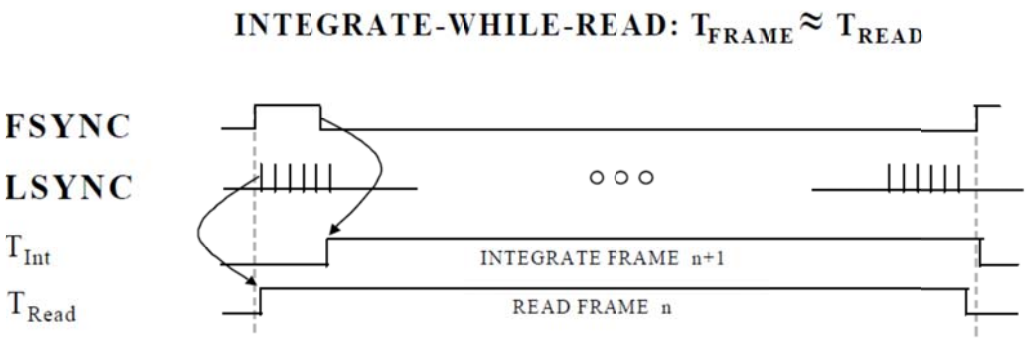


Figure 15 - Integrate While Read Timing

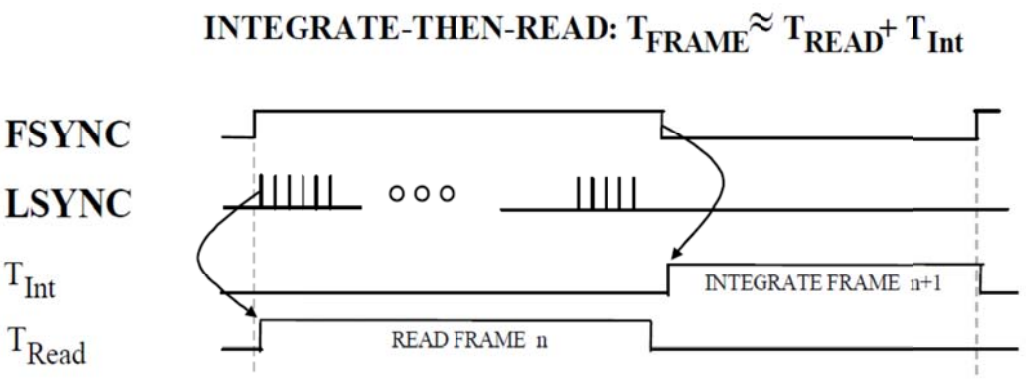


Figure 16 - Integrate Then Read Timing

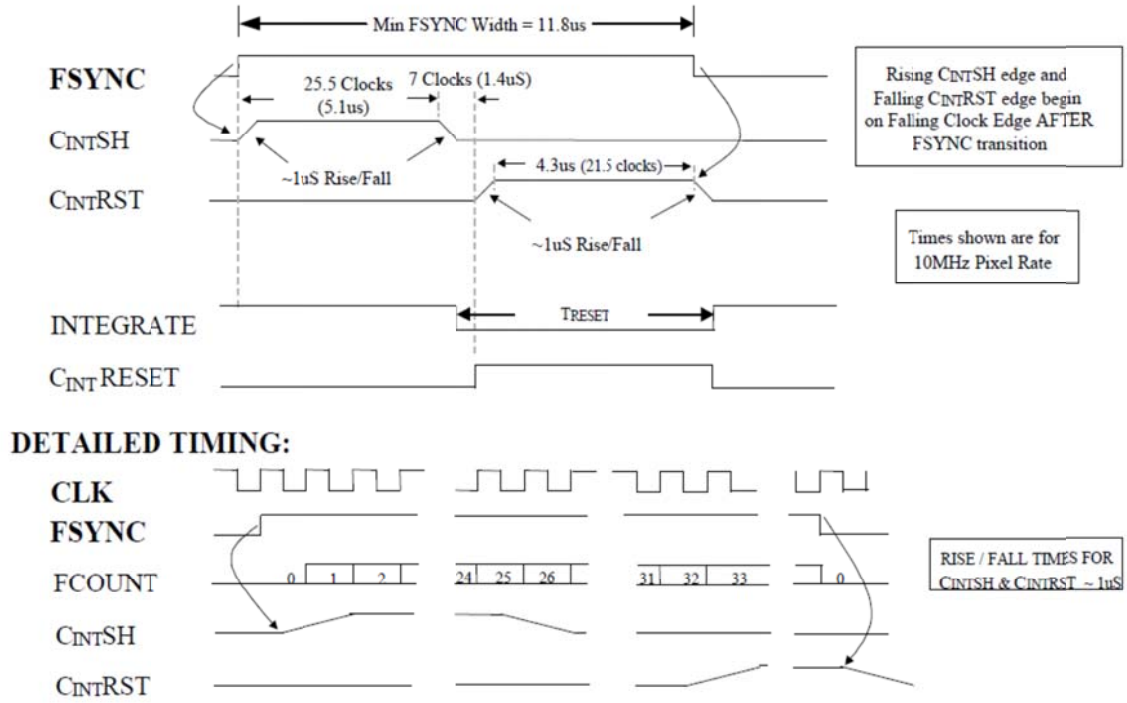


Figure 17 - FSYNC Timing Details

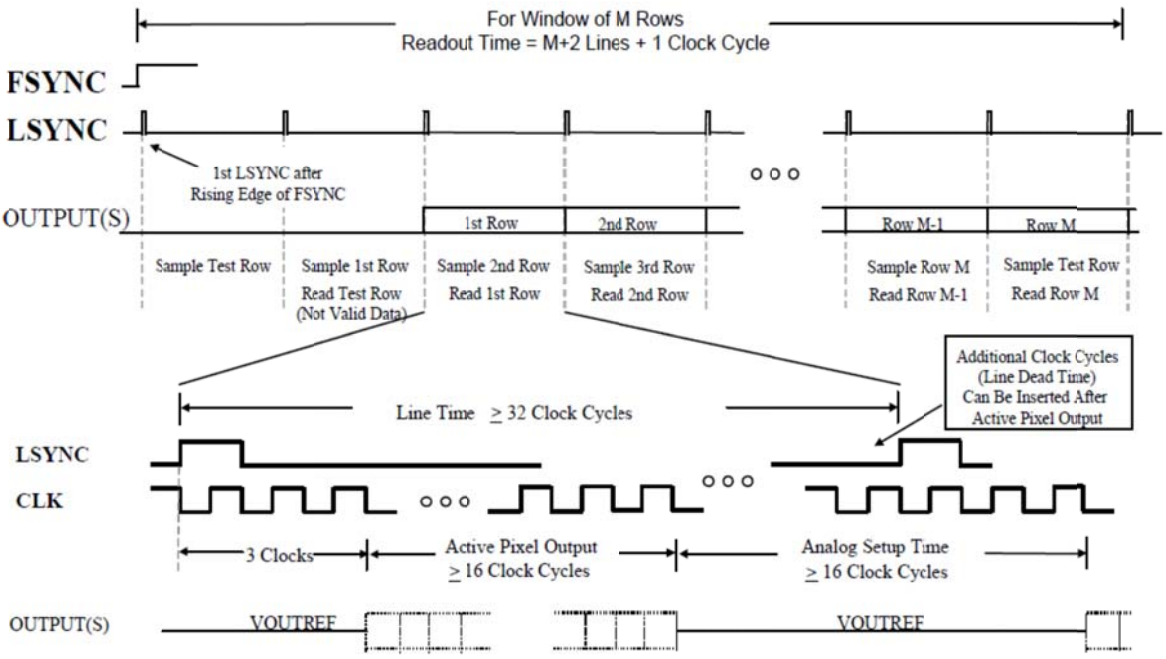


Figure 18 - LSYNC and Readout Timing Details

A simplified unit cell array is shown in **Figure 19**. Row selection lines have been highlighted in light blue while multiplexed column busses are shown in dark blue (other traces have been omitted for clarity). During frame readout, row selects are enabled in sequence, and unit cells associated with the selected row turn on their connections to the appropriate column bus. An array of transceivers exists on each end of the ROIC's column busses. They are grouped to form multiplexers that pass image and configuration data serially in and out of the ROIC. Shown in Figure 21, three I/O multiplexers are employed: the CTIA output multiplexer samples unit cell outputs and passes them to a analog output port; the detector bias demultiplexer accepts biasing information from the DET-BIAS input and uses it to refresh unit cell bias levels; and the CTIA gain demultiplexer performs a similar function for unit cell integration gain settings.

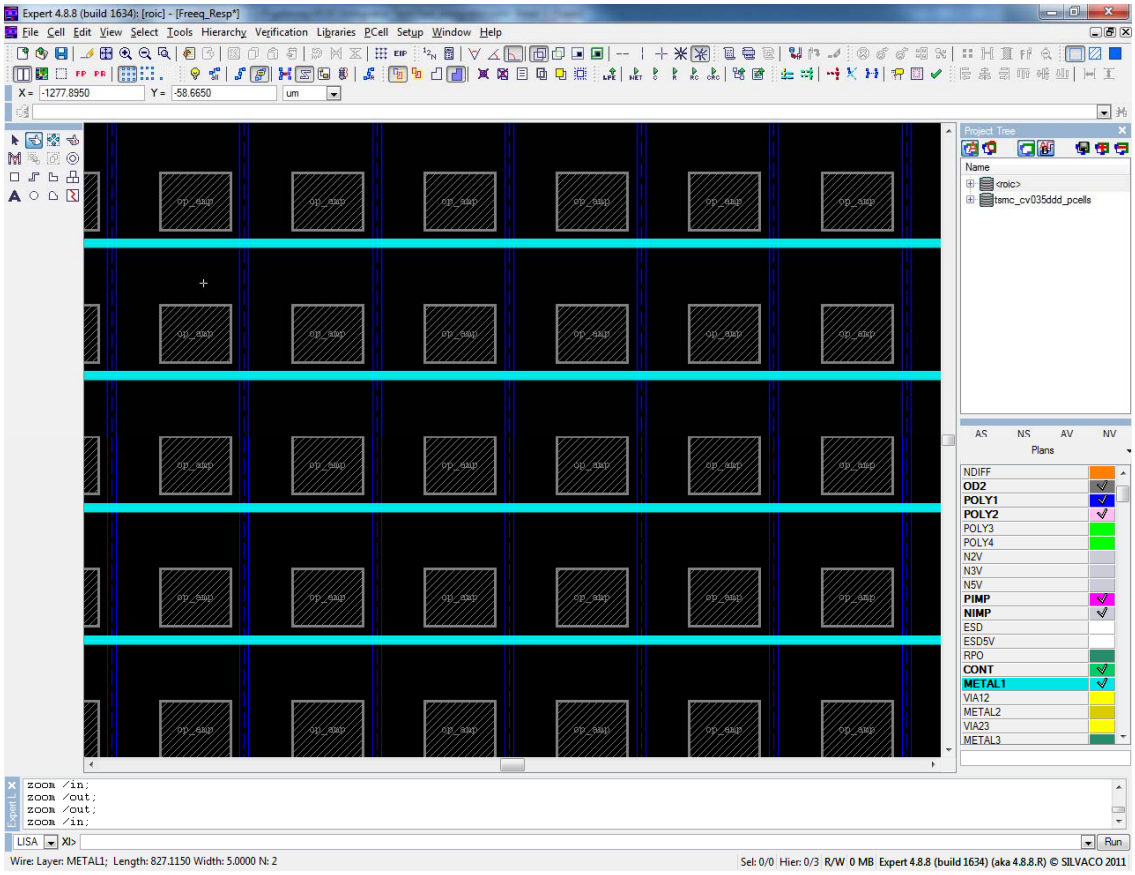


Figure 19 - Unit Cell Array Showing Row Select Lines and Multiplexed Column Busses

Figure 20 and 21 show high level schematics of the CTIA output multiplexer. It is composed of a single column sequencer, shown in **Figure 22**, and multiple column receivers, shown in **Figure 23**. The detector bias and integration gain demultiplexers use the same cells in their construction. However, receivers are reconfigured to support multiplexed signal flow into the ROIC.

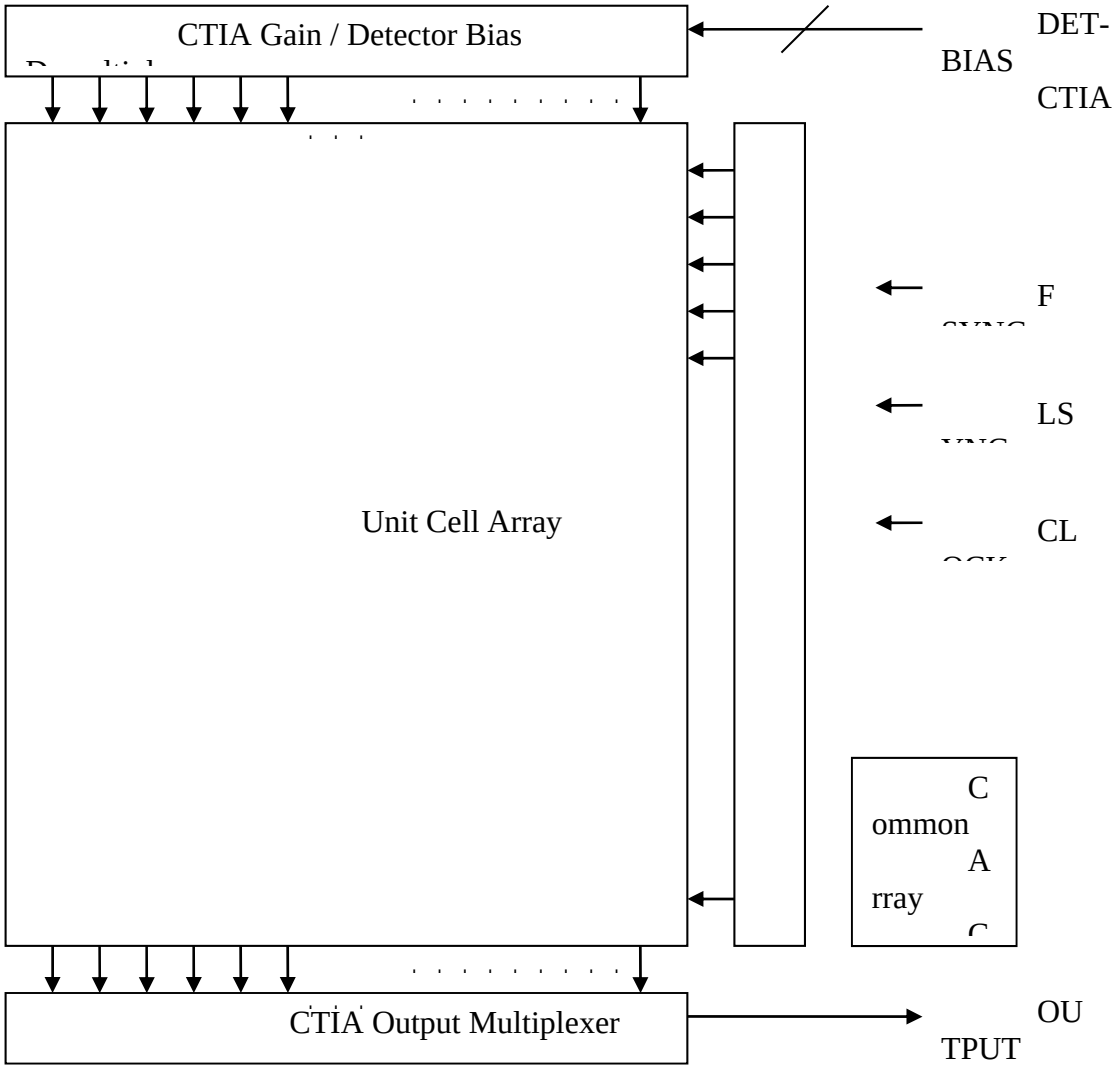


Figure 20 Multiplexer Assemblies Used in the ROIC

Row selection logic is implemented as a simple shift register. As seen in **Figure 24**, the rising edge of FSYNC marks the beginning of a new frame, and it is used to preset the row selection register so that it points to the first row of unit cells at the beginning of each frame. LSYNC is used to enable sampling of analog signals associated with the active row and to initiate processing of a new scan line by the column sequencer. The falling edge LSYNC is used to clock row selection logic so that it advances to the next row after analog sampling has been

completed. A hardware RESET will halt line scan processing and preset the row selection logic; placing the ROIC into an initialized state.

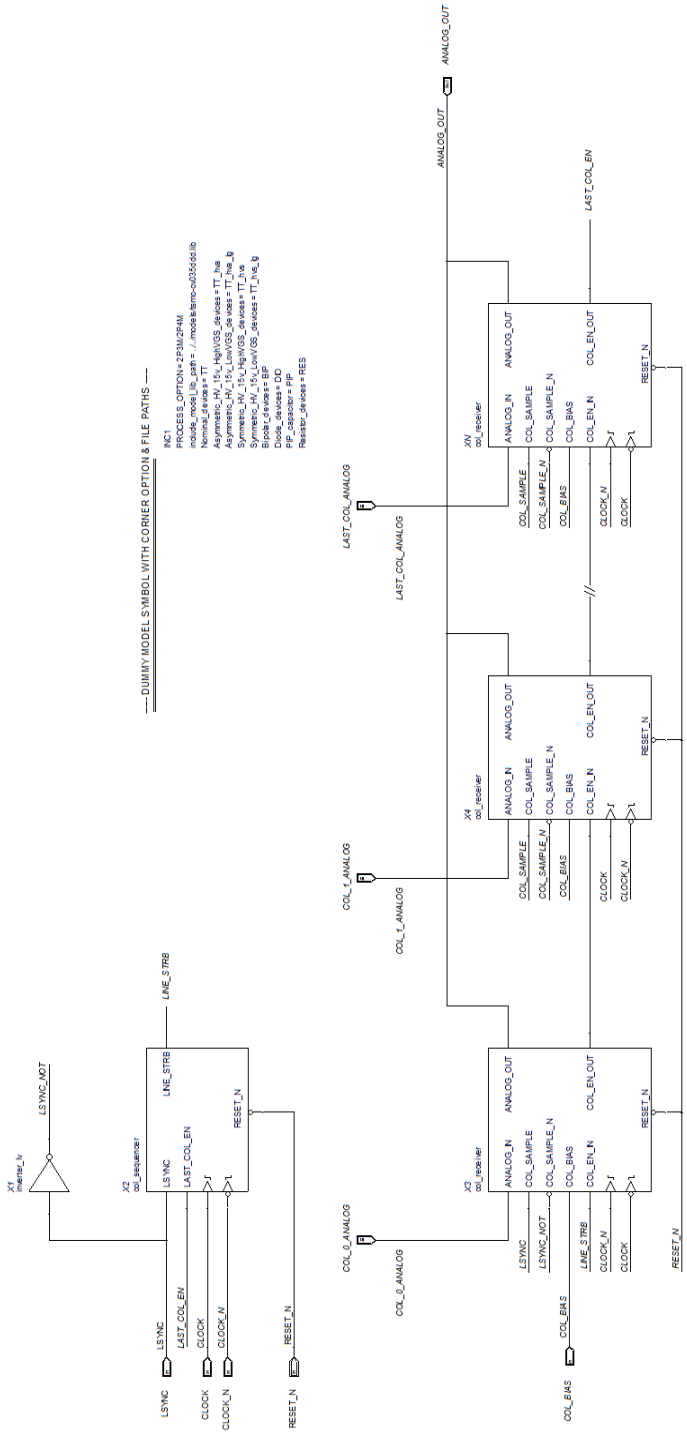


Figure 21 - CTIA Output Multiplexer

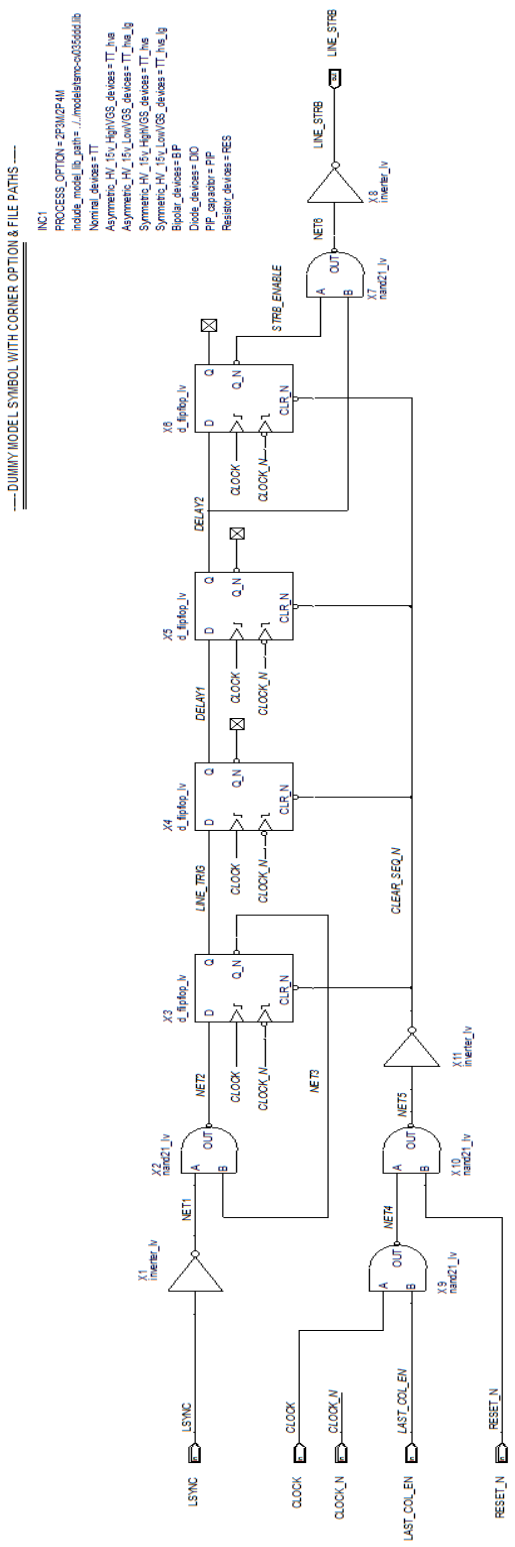


Figure 22- Column Readout Sequencer

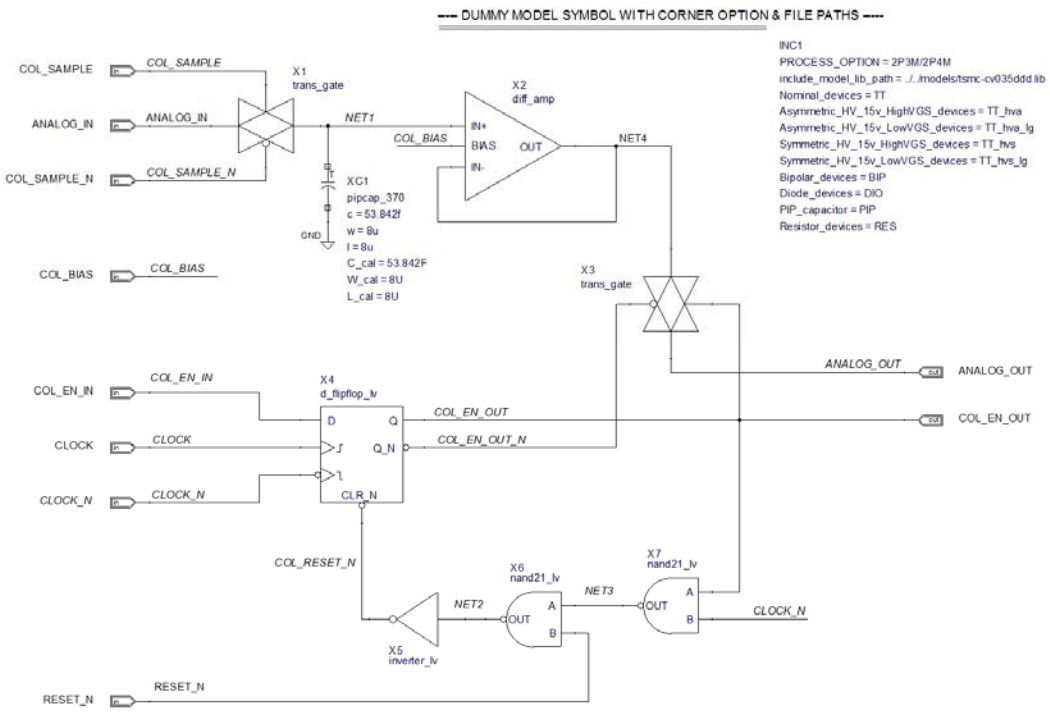


Figure 23 Column Receiver

Figure 24 shows the results of SPICE transient analysis performed to verify operation of the column readout sequencer and column receiver cell's tested in a CTIA multiplexer configuration. The top trace shows the reference input clock running at 10 MHz while the second trace shows the incoming LSYNC pulse. The third simulation window displays logic signals associated with a 3 clock delay which is inserted prior to the start of active pixel processing. The next three waveforms are associated with the first three ROIC column enables. For the purposes of testing, the number of array columns was limited to three. As a result, the readout sequencer's last column enable input is connected to the third column enable (col_2_en), and the sequencer is cleared after the third column has been enabled. It should be noted that the pixel update rate is twice the input clock rate as specified in **Figure 24's** timing diagram.

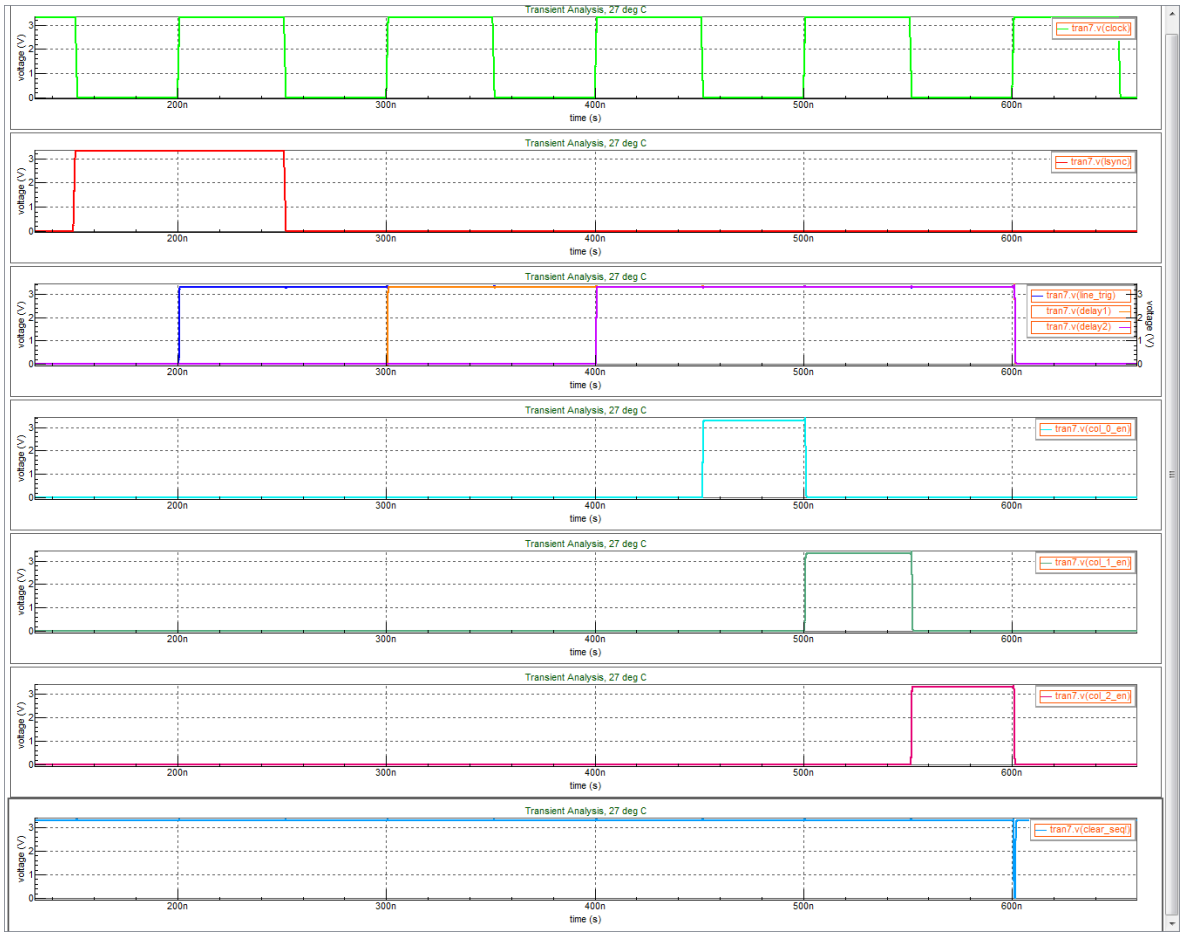


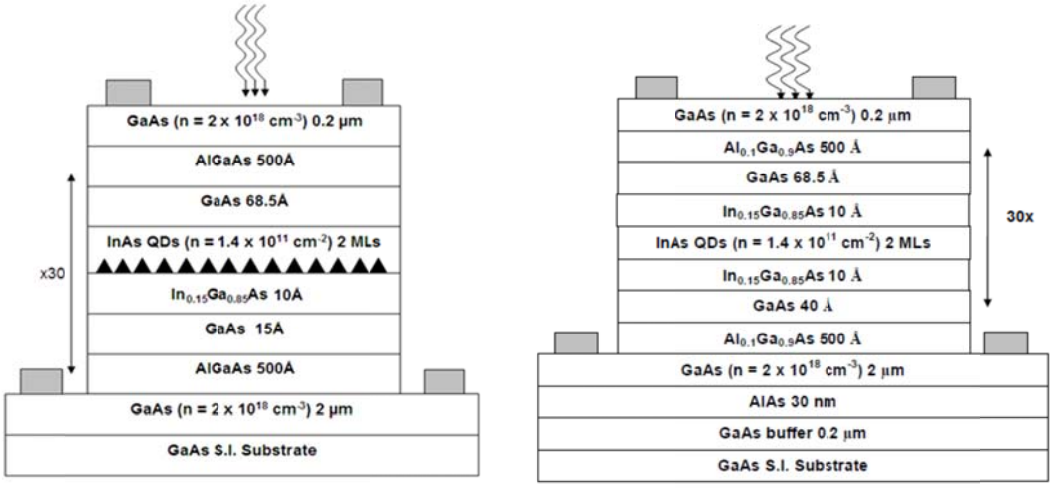
Figure 24 - Column Readout Sequencer Transient Analysis

4.2 Device measurements

[Intentionally left blank. This will be filled in with in the final report.]

4.3 DWELL Detector Design and Testing

A new class of infrared photodetectors, based on epitaxial quantum dots (QDs) have recently been proposed and developed. A key feature of this detector is that it exploits intersubband transitions between quantum-confined energy levels in a self-assembled dots-in-a-well (DWELL) structure in which QDs are embedded in a quantum well (QW) as shown in **Figure 25**.



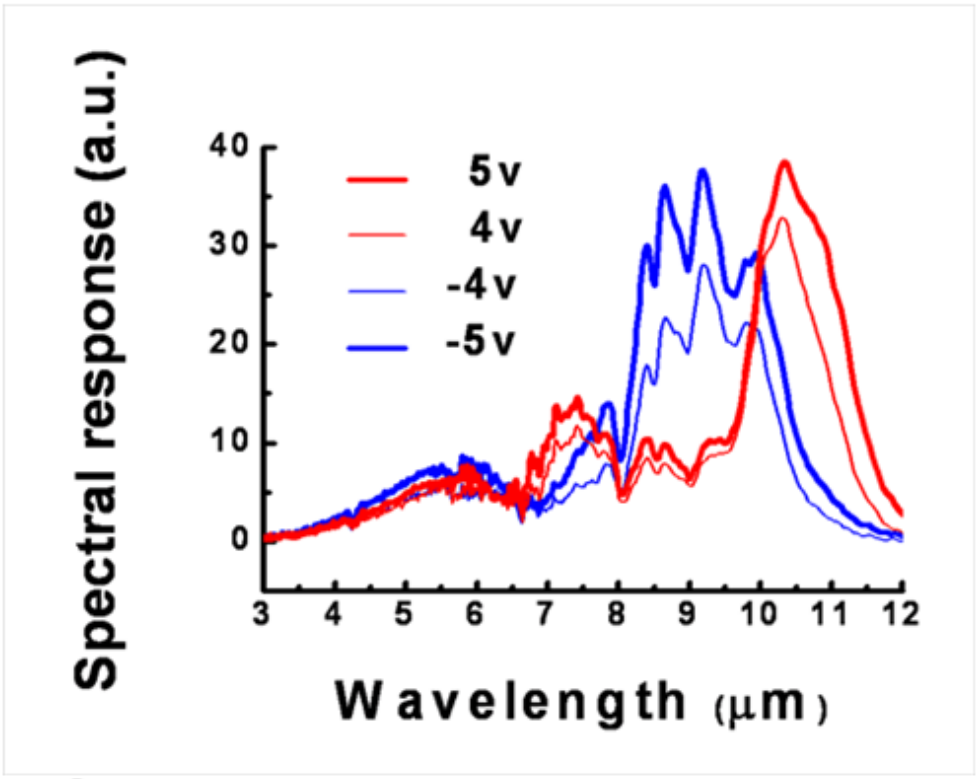
(a) (b)

Figure 25 Growth schematics of InAs/InGaAs/GaAs/AlGaAs DWELL heterostructures as shown in (a) and (b)

A DWELL structure is composed of InAs QDs (30 layers) embedded in an $In_{.15}Ga_{.85}As$ QW, the entire structure is then embedded in another GaAs QW with $Al_{.10}Ga_{.90}As$ barriers creating an InAs/InGaAs/GaAs/AlGaAs heterostructure between two n+ GaAs contact layers. Notable difference between two DWELL structures in **Figure 25** is the incremental change in the shoulder size of the GaAs well (from 15Å to 40Å) and the presence of shoulders on both sides of the InGaAs layer.

The DWELL photodetector offers operating-wavelength tailoring, inherent normal incidence operation, increased lifetime and three-dimensional quantum confinement. The operating wavelength is altered by varying the well width and material systems, which change the inter-sublevel transitions between energy levels (i.e., dot-to-dot, dot-to-well and dot-continuum (barrier) transitions) in a DWELL structure. Additionally, the spectral response of DWELL photodetector is continuously tuned by means of varying applied bias voltages without any optical filters. This electrical tunability is due to the quantum-confined Stark effect, depending upon the asymmetric electronic potential of a geometrically asymmetric DWELL structure. Two main attributes of this geometry are the shape of the dot and the different thicknesses of the QW above and below the dot, which together lead to variation of the local potential as a function of the applied bias. As a result, a single bias-tunable DWELL

photodetector can be performed as a multispectral photodetector albeit with overlapping spectral responses.



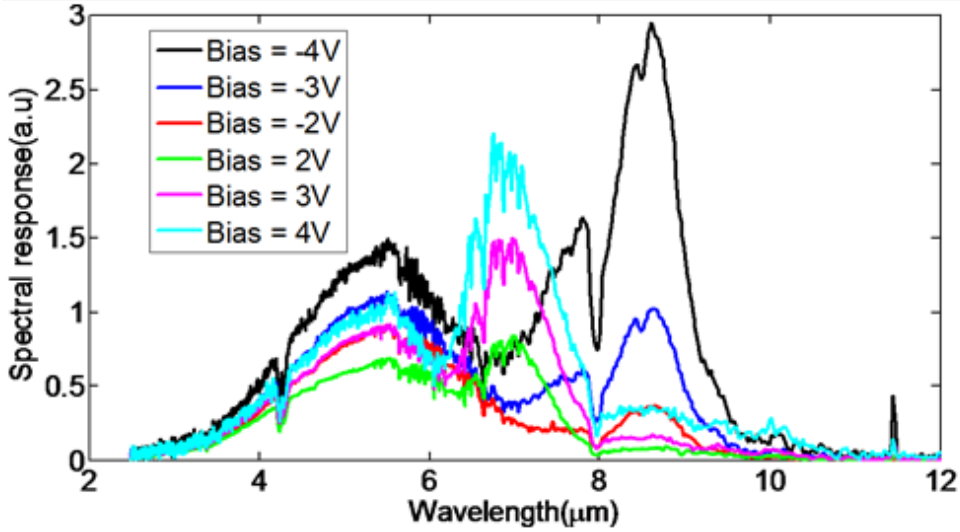


Figure 26 Bias-dependent spectral responses of (Top) the DWELL structure shown in Fig. 1 (a) at 60 K device temperature and (bottom) DWELL structure shown in Fig. 1 (b) at 100 K device temperature for various applied bias voltages

5.0 CONCLUSIONS

Polaris Sensor Technologies and UNM have completed a design for a ROIC chip that can be used to control a DWELL Quantum Dot FPA to apply bias voltages to the FPA pixels individually so that the FPA can be operated as a spatially spectrally agile LWIR sensor. The ROIC can supply bias voltages to individual pixels of up to +/- 5 Volts. The design has been submitted to MOSIS prototyping foundry for fabrication. Due to foundry delays the chip will not be completed until 15Jul 2012. When the chip is completed, it will be tested by UNM and the test results will be added to Section 4.2 of this report. The Final Report will be submitted by 31 Jul 2012.

A DWELL device was fabricated and tested in this effort to demonstrate its spectral agility. Shifts in spectral peak of as much as 2 microns were achieved for bias shifts of +/- 5 volts. Although an individually addressable quantum dot focal plane array was not demonstrated, the risk assessment for the technology was significantly reduced as a result of this program. Spatially addressable ROIC with pixel level bias control is one of the major achievements of this effort.

6.0 RECOMMENDATIONS

Once the ROIC has been tested and validated that it works, we recommend that a Spectrally Agile LWIR camera be built based on the DWELL FPA and ROIC. This would require a follow on funding to accomplish this task. We believe that this SBIR program has taken an important step in the grand vision of multimodal sensors in which enhanced functionality such as spectral agility is encoded in the pixel level.

LIST OF SYMBOLS, ABBREVIATIONS, AND ACRONYMS

CMOS	COMPLIMENTARY – SYMMETRY METAL OXIDE SEMICONDUCTOR
CTIA	CAPACITIVE TRANSIMPEDANCE AMPLIFIER
DWELL	DOTS IN A WELL
ESD	ELECTRO STATIC DISCHARGE
FPA	FOCAL PLANE ARRAY
FSYNC	FRAME SYNC SIGNAL
LYNC	LINE SYNC SIGNAL
LWIR	LONG WAVE INFRARED
MOFSET	METAL-OXIDE-SEMICONDUCTOR FIELD EFFECT TRANSISTOR
MWIR	MIDWAVE INFRARED
QD	QUANTUM DOTS
QW	QUANTUM WELLS
ROIC	READOUT INTEGRATED CIRCUITS
SPICE	SIMULATION PROGRAM WITH INTEGRATED CIRCUIT EMPHASIS
TSMC	TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY
UNM	UNIVERSITY OF NEW MEXICO